

Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT
 (Autonomous Institute under Visvesvaraya Technological University, Belagavi)

2022 SCHEME

USN

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Course Code

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Sixth Semester B.E. Degree Examinations, May/June 2026

EMBEDDED SYSTEM DESIGN

Duration: 3 hrs

Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. Missing data, if any, may be suitably assumed

<u>Q. No</u>	<u>Question</u>	<u>Marks</u>	<u>(RBTl:CO: PI)</u>
<u>Module-1</u>			
1.	a. Define an instruction. Describe the actions involved in executing an instruction with examples.	10	(2:1:1.6.1)
	b. List and explain the classification of real time embedded system with examples.	10	(2:1:1.6.1)
(OR)			
2.	a. With a block diagram, explain the microprocessor based embedded system.	10	(2:1:1.6.1)
	b. With the neat flow chart, explain the process of embedded system design and development.	10	(2:1:1.6.1)
<u>Module-2</u>			
3.	a. Explain the array organization of a simple memory model and describe the common memory control signals	10	(2:2:1.6.1)
	b. Explain the typical internal architecture of a memory chip and describe the concept of a basic memory map.	10	(2:2:1.6.1)
(OR)			
4.	a. Illustrate and explain the three operational states of SRAM using suitable block and timing diagrams.	10	(2:2:1.6.1)
	b. With the neat circuit and timing diagram, explain the inside and outside overview of ROM.	10	(2:2:1.6.1)
<u>Module-3</u>			
5.	a. With the neat interface diagram, explain on-board I ² C communication bus.	10	(2:3:1.6.1)
	b. Compare embedded systems with general computing systems. Also, list the major application areas of embedded systems.	10	(2:3:1.6.1)
(OR)			
6.	a. With a neat architectural diagram, describe the concept of load store operation.	10	(2:3:1.6.1)
	b. Differentiate between	10	(2:3:1.6.1)
	(i) Microprocessor and Microcontroller		
	(ii) Big Endian and Little Endian		

Note: (RBTl - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI- Performance Indicator)

Module-4

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| 7. | a. | Define life cycle model and its objectives. With the neat diagram, explain waterfall life- cycle model. | 10 | (2:4:1.6.1) |
| | b. | Illustrate and explain the spiral life cycle model using a suitable diagram. | 10 | (2:4:1.6.1) |

(OR)

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| 8. | a. | With neat illustration, describe the different phases of the V-model. | 10 | (2:4:1.6.1) |
| | b. | Identify and describe the five steps of a successful embedded system design process. | 10 | (2:4:1.6.1) |

Module-5

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| 9. | a. | Considering the example model, describe single and multiple processes in the embedded system design. | 10 | (2:5:1.6.1) |
| | b. | With a neat block diagram and C code fragment, Explain the Task control block | 10 | (2:5:1.6.1) |

(OR)

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| 10. | a. | Explain the following
(i) Task and Things
(ii) Program and Processes | 10 | (2:5:1.6.1) |
| | b. | With a neat block diagram, Explain the major components of operating system. | 10 | (2:5:1.6.1) |

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